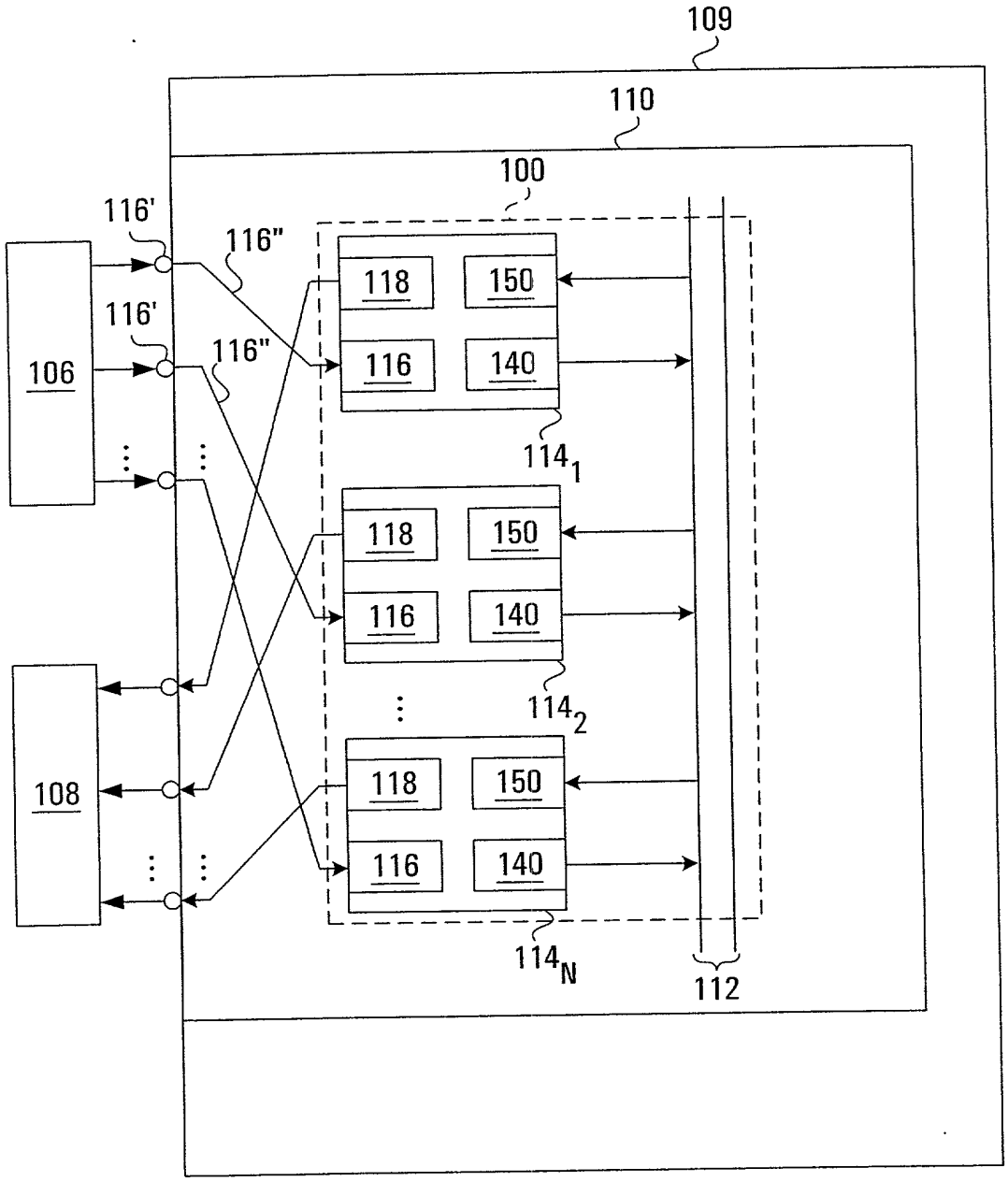

109
110
100
116'
116"
116'
116"
106
118
150
116
140
114_1
118
150
116
140
114_2
108
118
150
116
140
114_N
112

FIG. 1

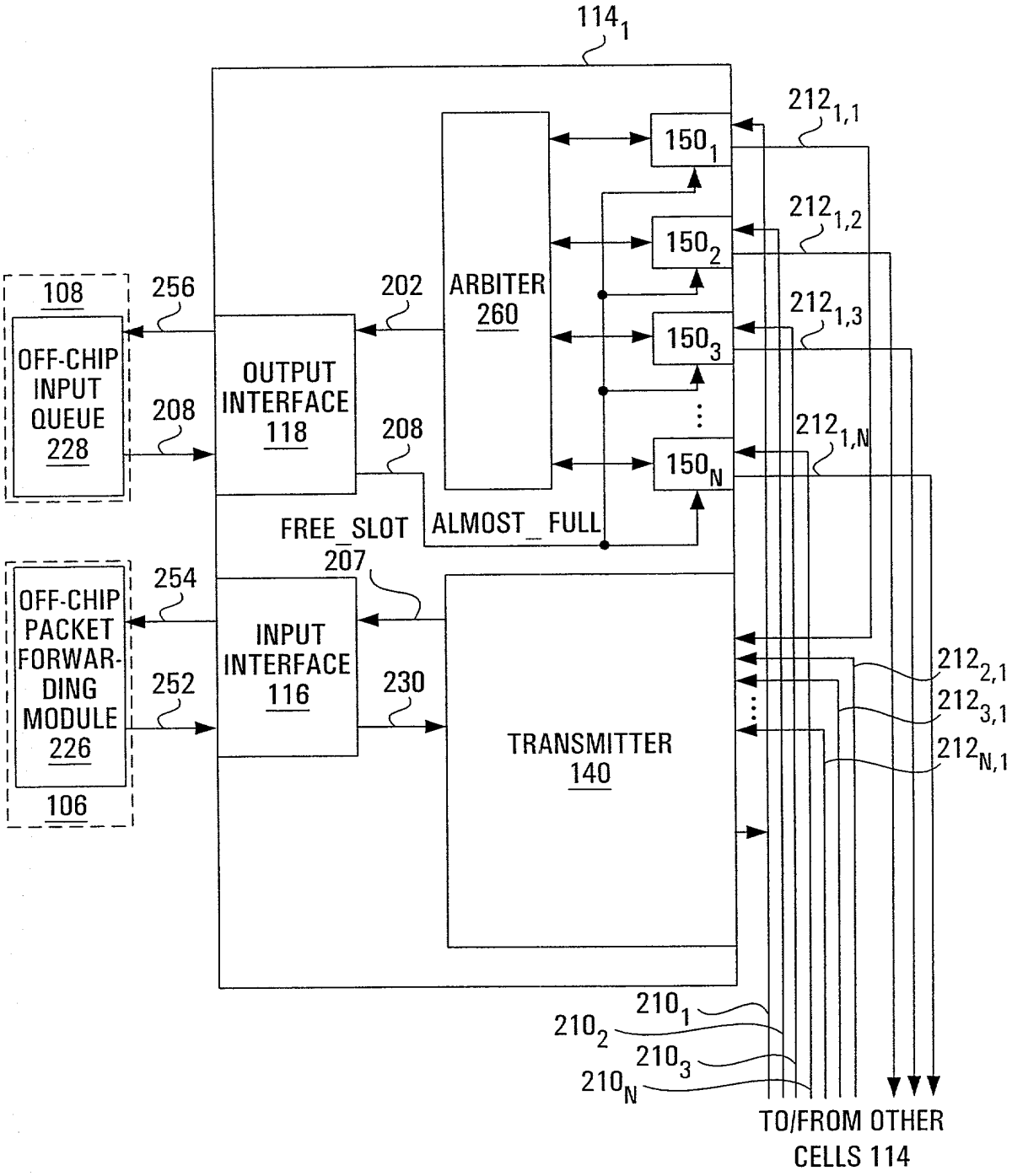

114 1
212 1,1
150 1
212 1,2
150 2
212 1,3
150 3
212 1,N
150 N
ARBITER 260
202
108
256
OFF-CHIP INPUT QUEUE 228
208
OUTPUT INTERFACE 118
208
FREE_SLOT
ALMOST_FULL
207
254
OFF-CHIP PACKET FORWAR-DING MODULE 226
252
INPUT INTERFACE 116
230
TRANSMITTER 140
106
212 2,1
212 3,1
212 N,1
210 1
210 2
210 3
210 N
TO/FROM OTHER CELLS 114

FIG. 2

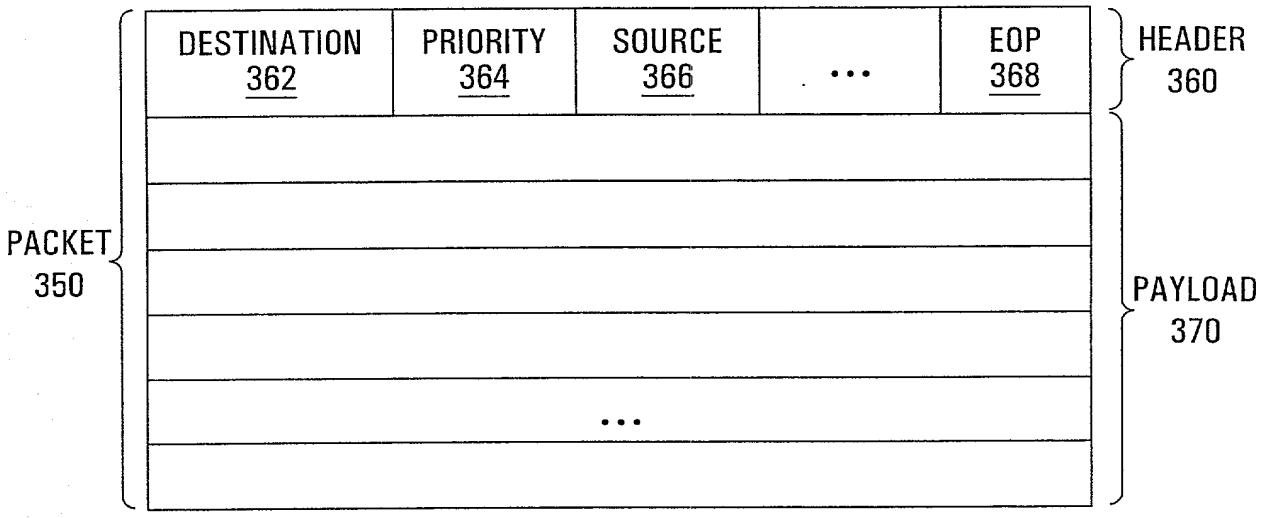


FIG. 3

WO 2004/088470 PCT/US2004/007470

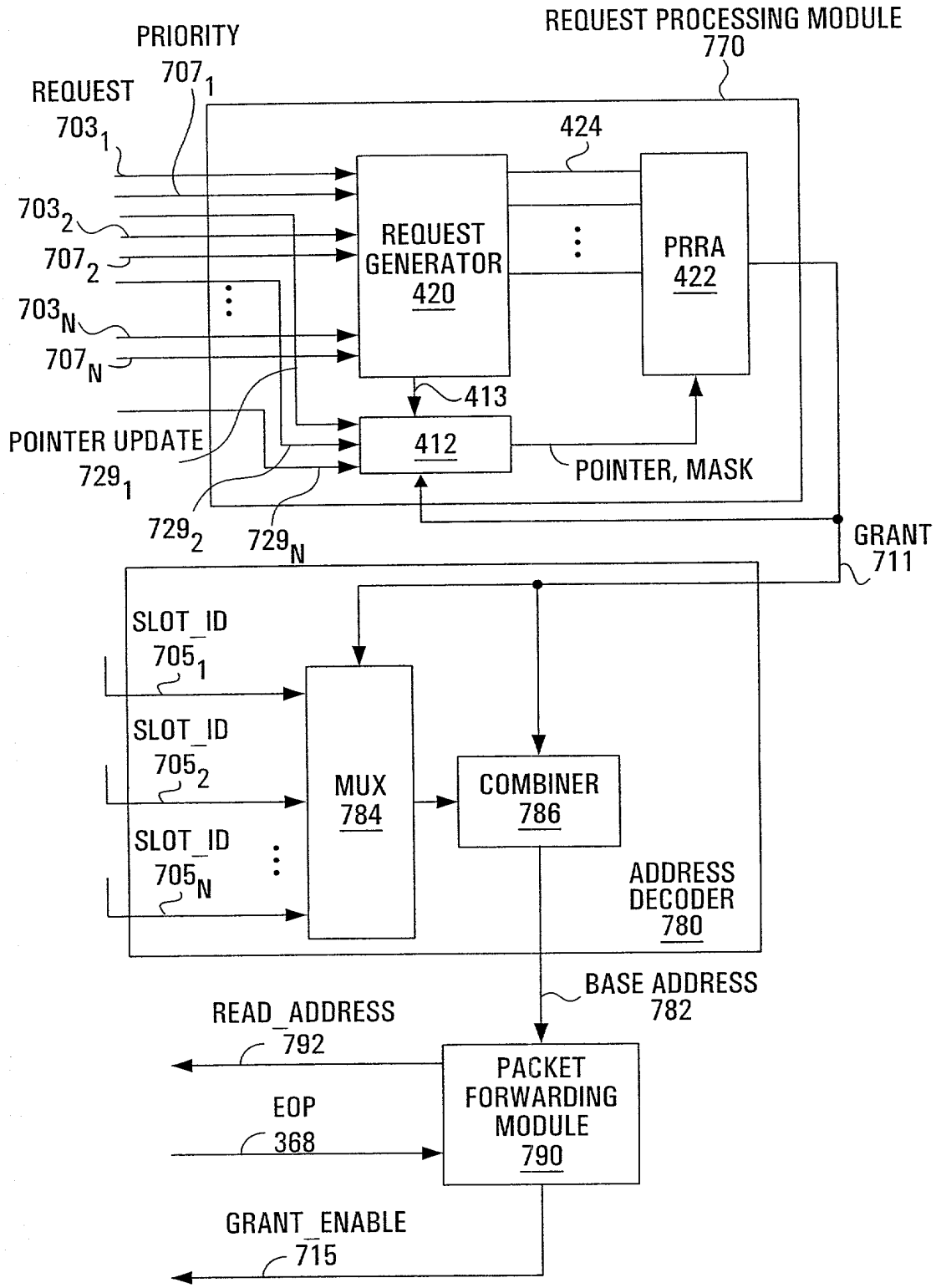

REQUEST PROCESSING MODULE
770
PRIORITY
707_1
REQUEST
703_1
424
703_2
707_2
REQUEST GENERATOR
420
PRRA
422
703_N
707_N
413
POINTER UPDATE
729_1
412
POINTER, MASK
729_2
729_N
GRANT
711
SLOT_ID
705_1
SLOT_ID
705_2
SLOT_ID
705_N
MUX
784
COMBINER
786
ADDRESS DECODER
780
BASE ADDRESS
782
READ_ADDRESS
792
PACKET FORWARDING MODULE
790
EOP
368
GRANT_ENABLE
715

FIG. 4

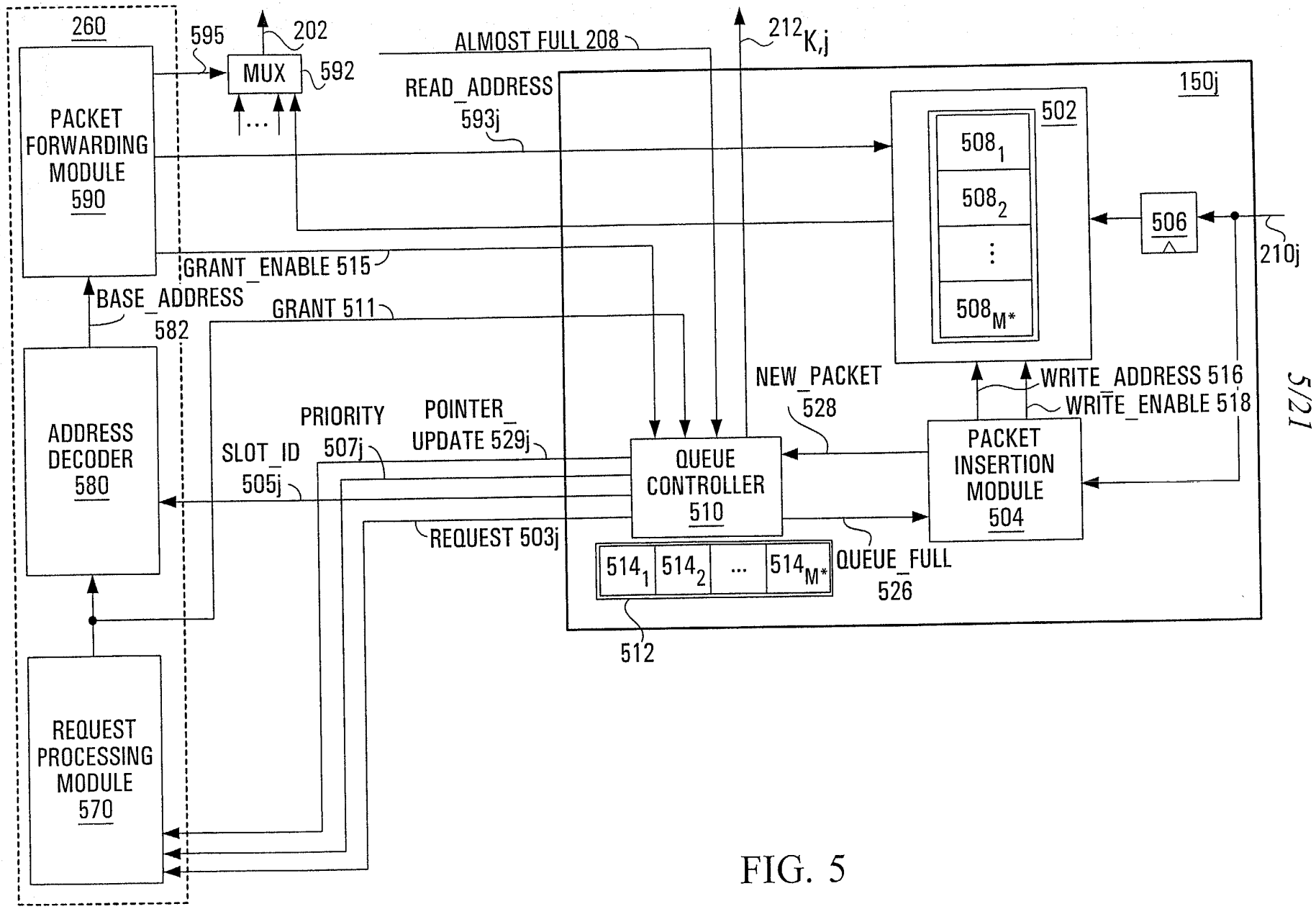

260
595
202
MUX
592
ALMOST FULL 208
212 K,j
150j
PACKET FORWARDING MODULE 590
READ_ADDRESS 593j
502
508 1
508 2
508 M*
506
210j
GRANT_ENABLE 515
BASE_ADDRESS 582
GRANT 511
NEW_PACKET 528
WRITE_ADDRESS 516
WRITE_ENABLE 518
ADDRESS DECODER 580
PRIORITY 507j
POINTER_ UPDATE 529j
SLOT_ID 505j
QUEUE CONTROLLER 510
PACKET INSERTION MODULE 504
REQUEST 503j
514 1
514 2
514 M*
QUEUE_FULL 526
512
REQUEST PROCESSING MODULE 570

FIG. 5

5/21

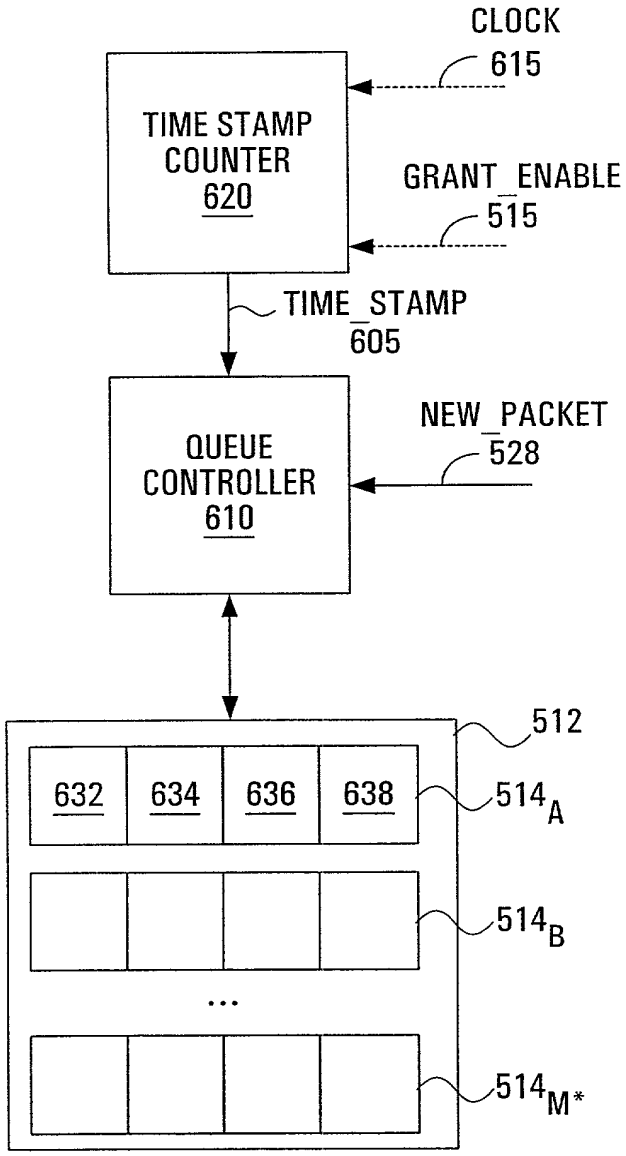

CLOCK
615
TIME STAMP
COUNTER
620
GRANT_ENABLE
515
TIME_STAMP
605
QUEUE
CONTROLLER
610
NEW_PACKET
528
512
632
634
636
638
514A
514B
...
514M*

FIG. 6

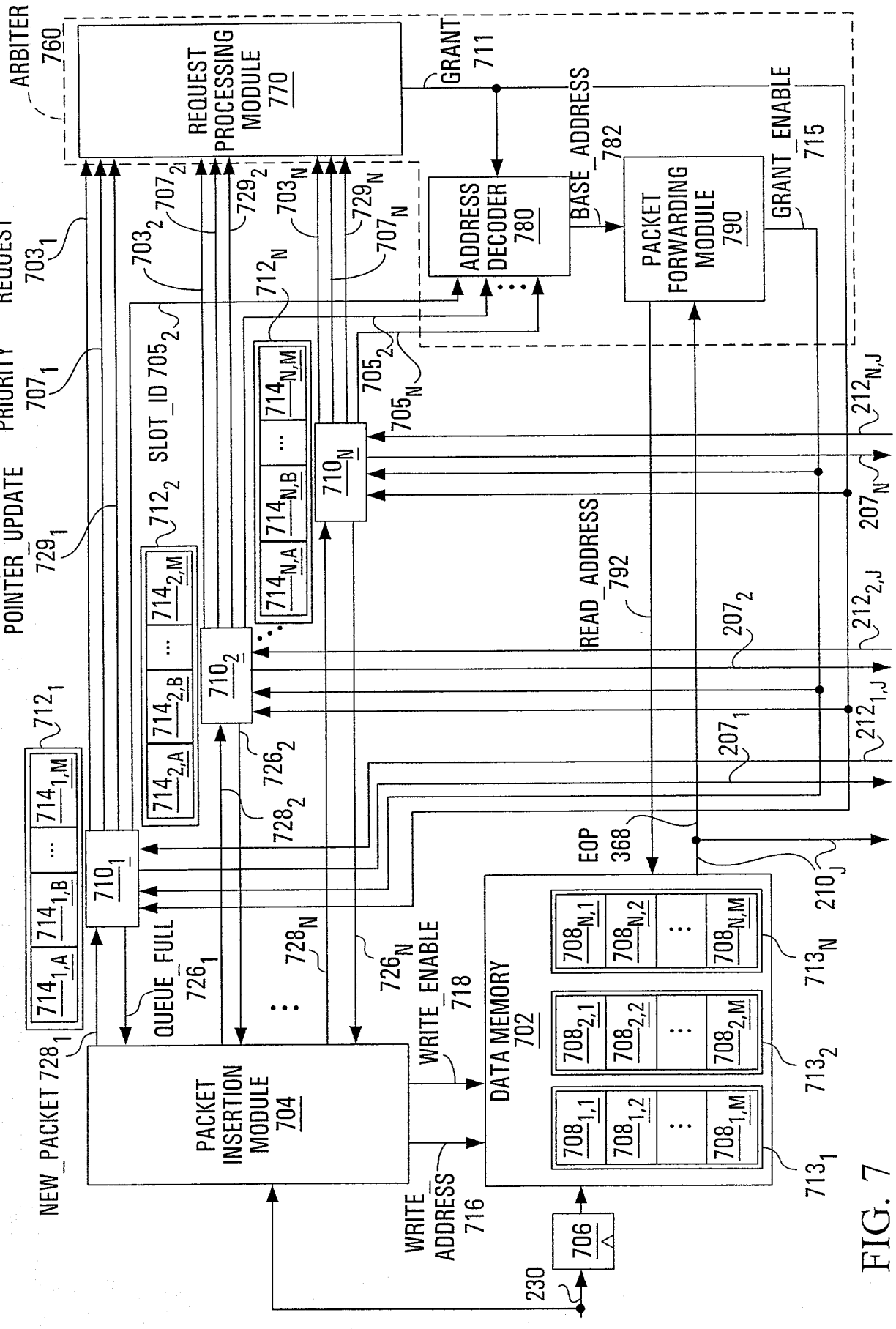

ARBITER 760
REQUEST PROCESSING MODULE 770
GRANT 711
ADDRESS DECODER 780
BASE_ADDRESS 782
PACKET FORWARDING MODULE 790
GRANT_ENABLE 715
REQUEST 703
PRIORITY 707
POINTER_UPDATE 729
SLOT_ID 705
NEW_PACKET 728
QUEUE_FULL 726
WRITE_ENABLE 718
WRITE_ADDRESS 716
PACKET INSERTION MODULE 704
DATA MEMORY 702
READ_ADDRESS 792
EOP 368
706
230

FIG. 7

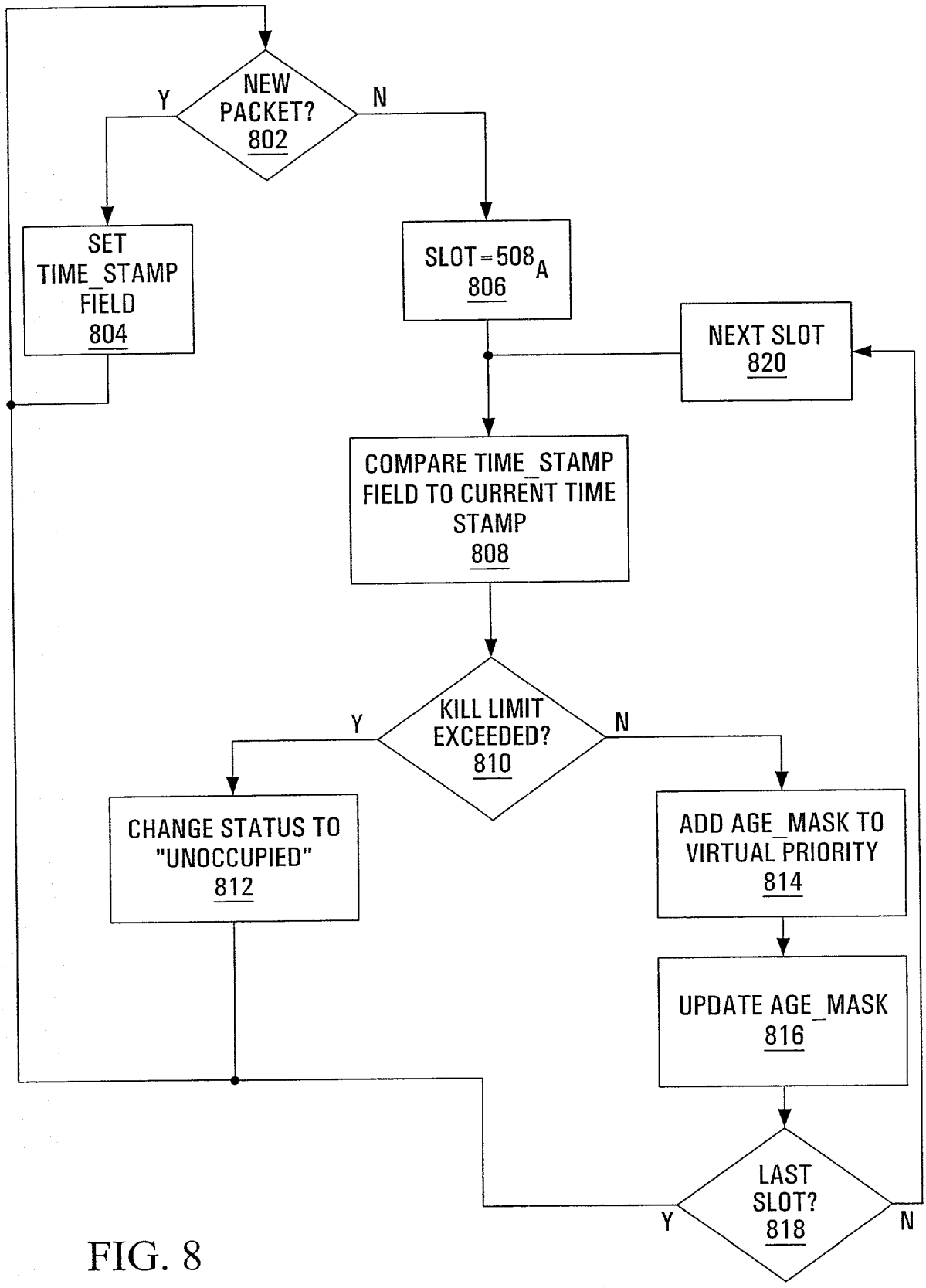

NEW PACKET? 802
Y
N
SET TIME_STAMP FIELD 804
SLOT=508A 806
NEXT SLOT 820
COMPARE TIME_STAMP FIELD TO CURRENT TIME STAMP 808
KILL LIMIT EXCEEDED? 810
Y
N
CHANGE STATUS TO "UNOCCUPIED" 812
ADD AGE_MASK TO VIRTUAL PRIORITY 814
UPDATE AGE_MASK 816
LAST SLOT? 818
Y
N

FIG. 8

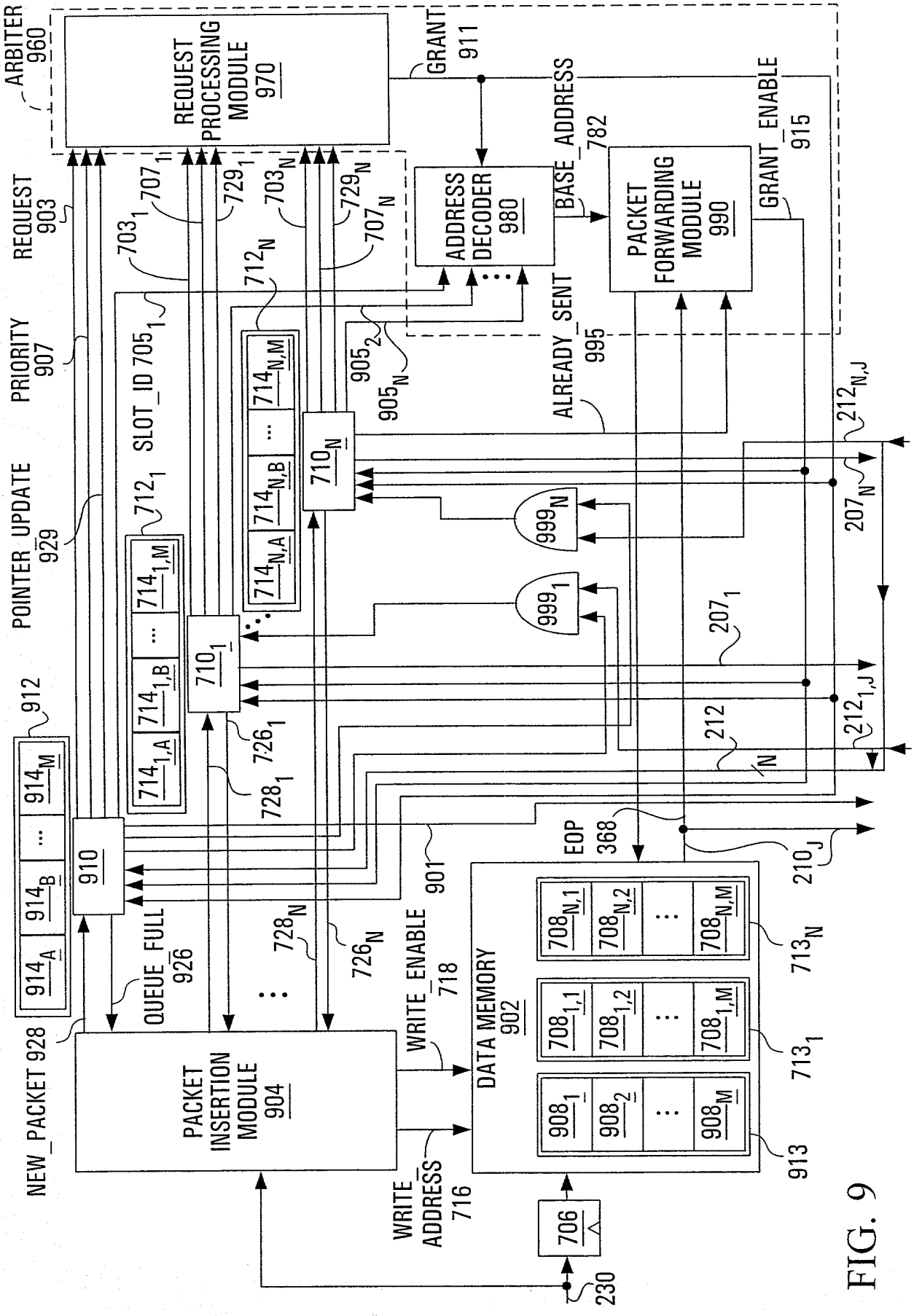

ARBITER 960
REQUEST PROCESSING MODULE 970
GRANT 911
REQUEST 903
PRIORITY 907
POINTER_UPDATE 929
SLOT_ID 705
ADDRESS DECODER 980
BASE_ADDRESS 782
PACKET FORWARDING MODULE 990
GRANT_ENABLE 915
ALREADY_SENT 995
NEW_PACKET 928
QUEUE_FULL 926
WRITE_ENABLE 718
WRITE_ADDRESS 716
EOP 368
PACKET INSERTION MODULE 904
DATA MEMORY 902
910
912
706
230
901
913

FIG. 9

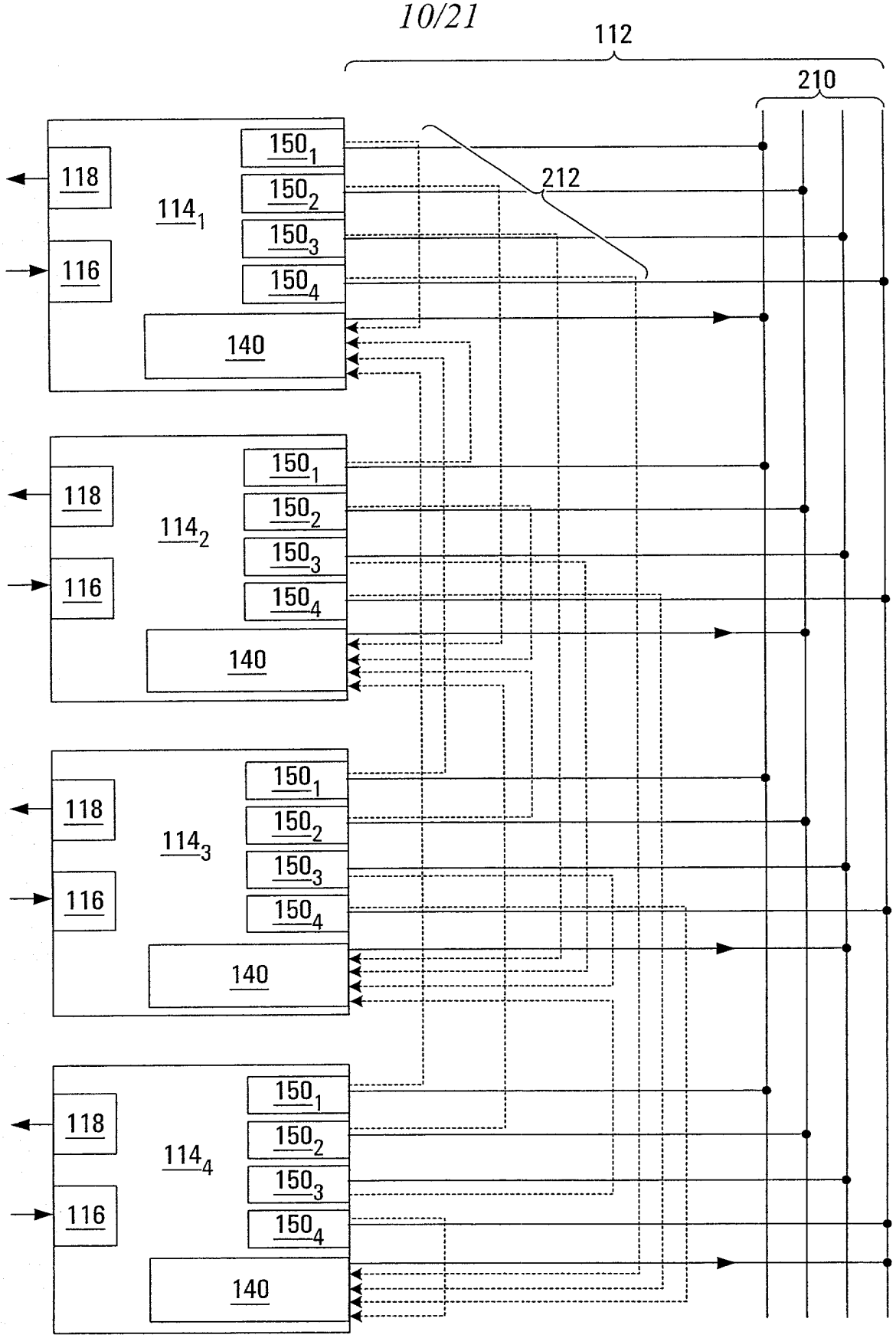

112
210
212
150_1
150_2
150_3
150_4
118
116
140
114_1
114_2
114_3
114_4

FIG. 10

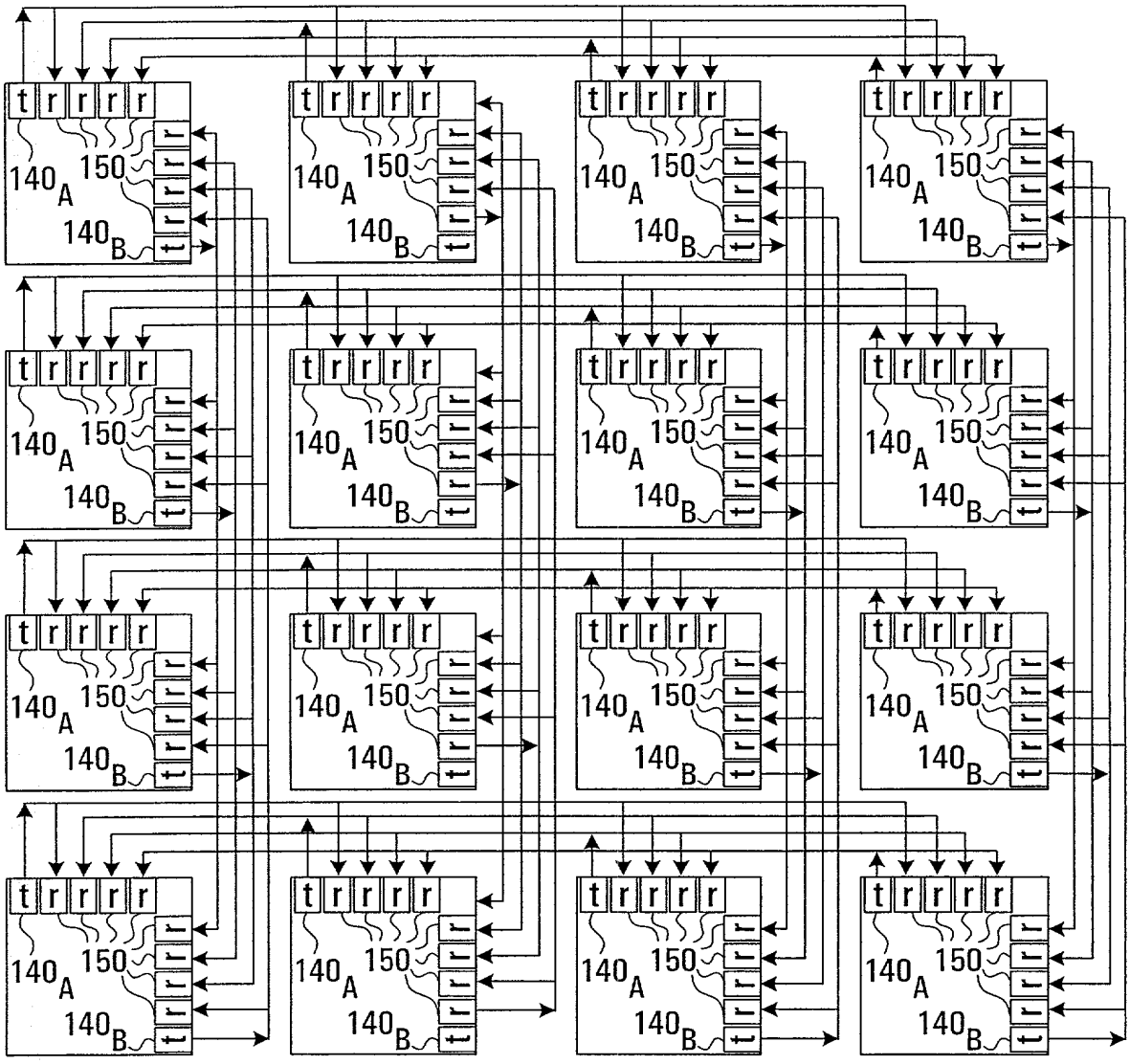


FIG. 11

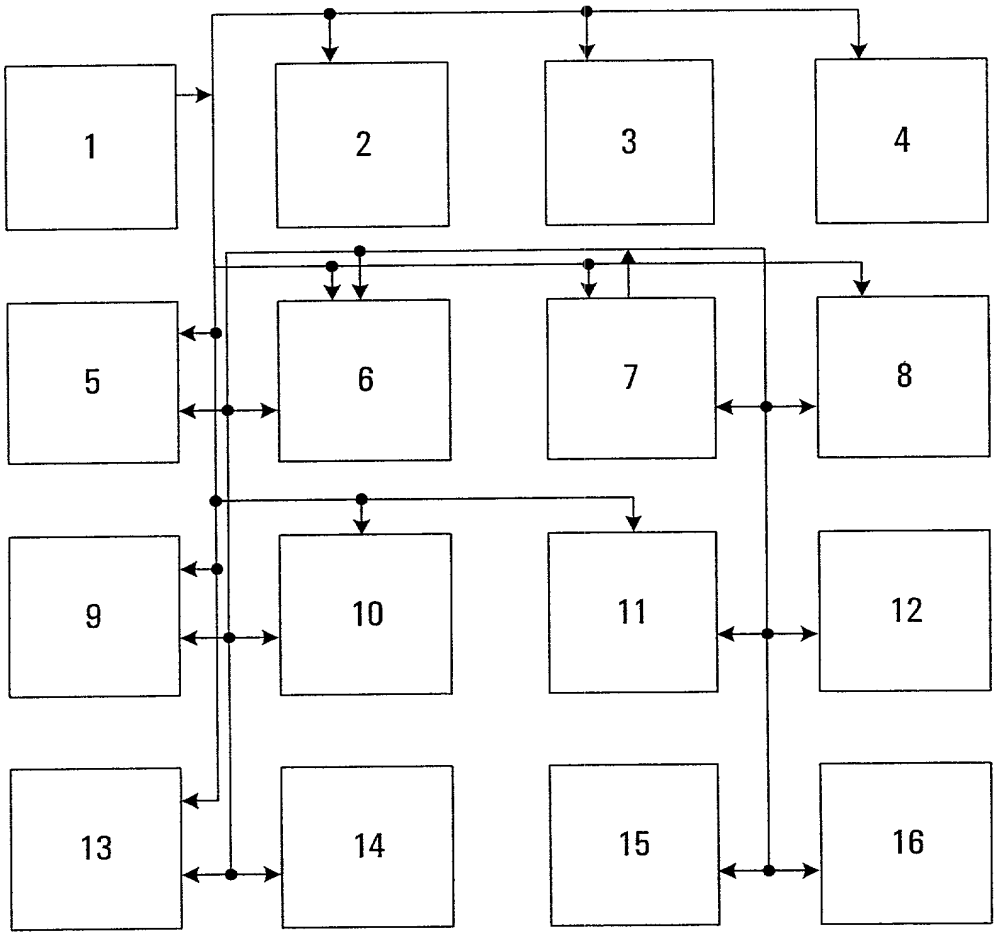


FIG. 12

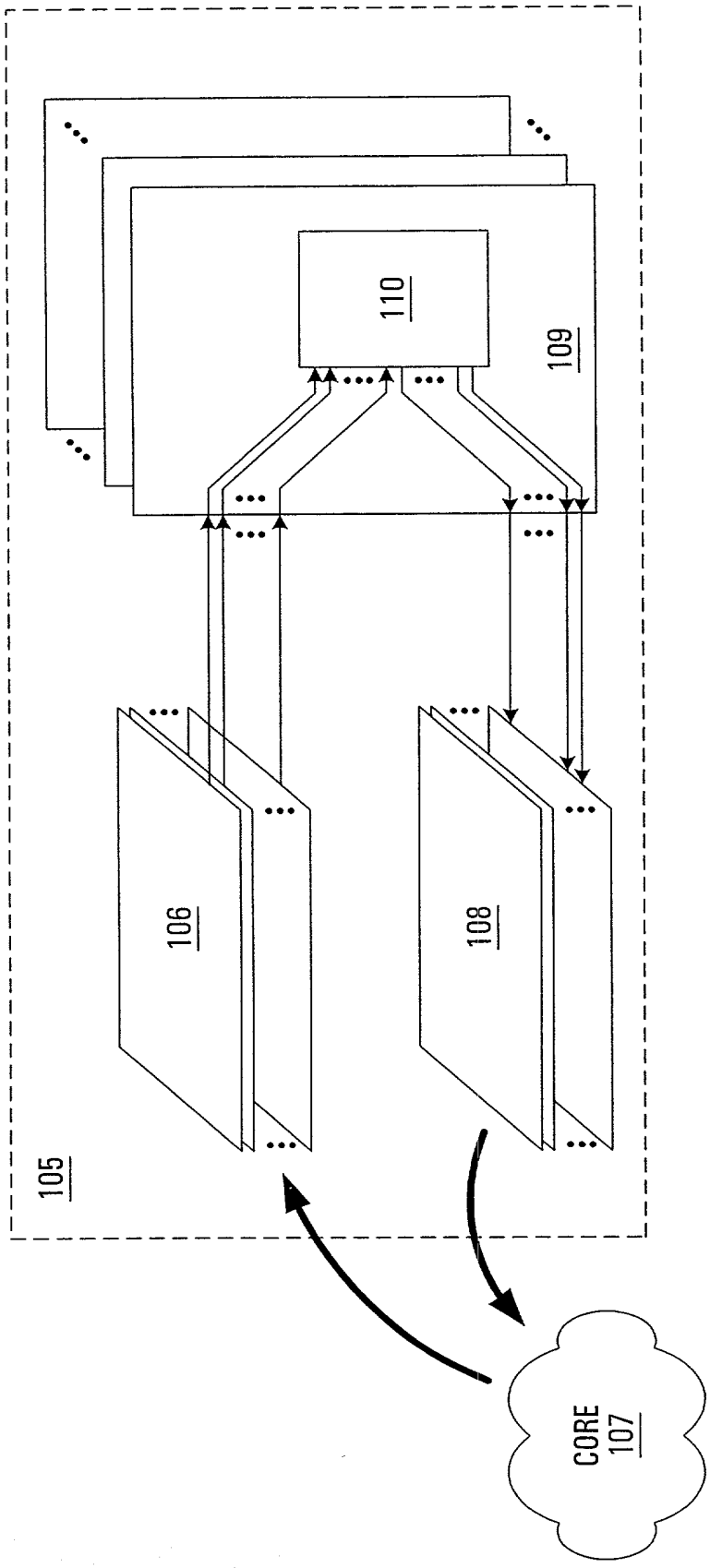


FIG. 13

EP 2 510 080 A4

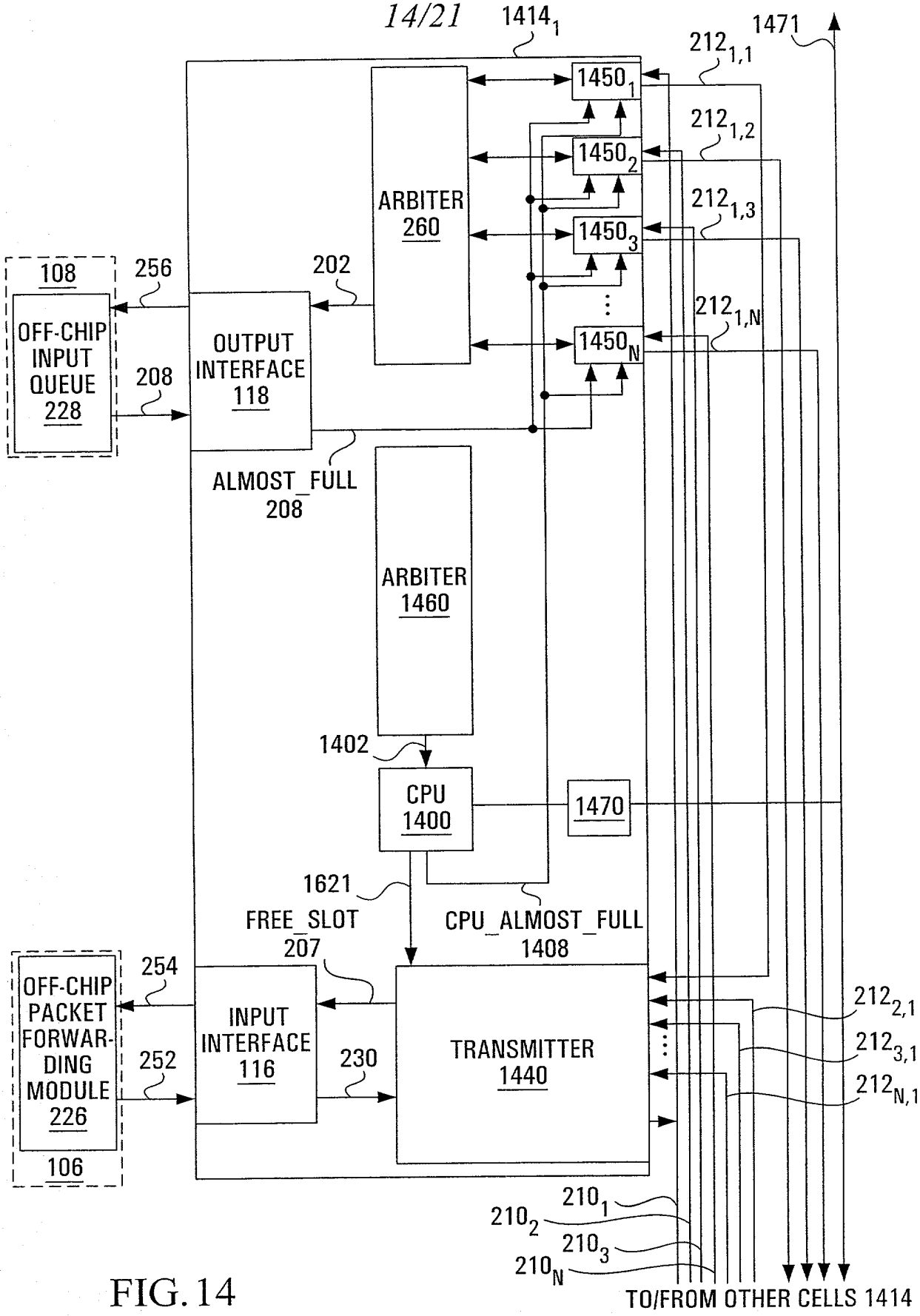


FIG. 14

EP 1 959 629 A2

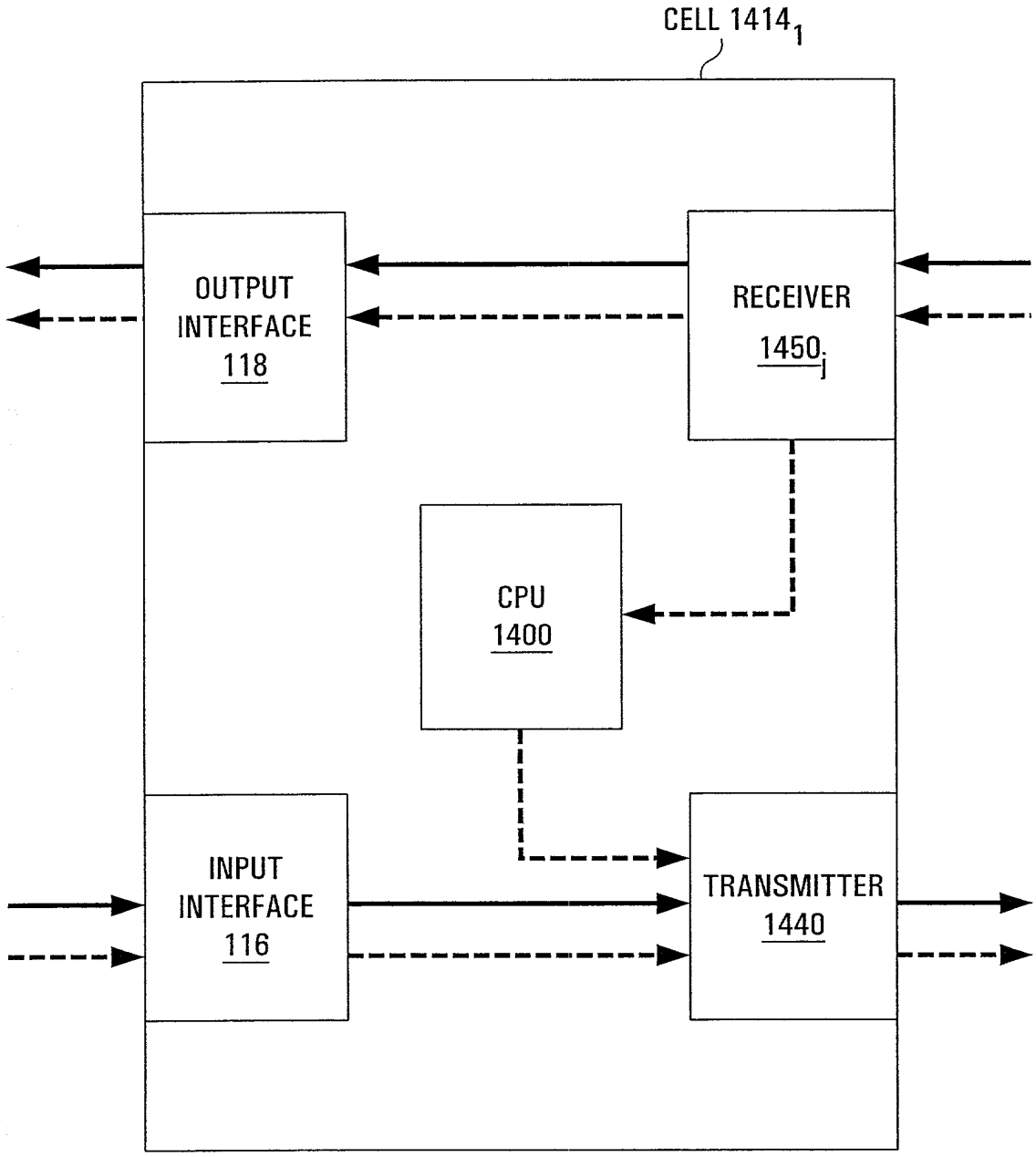

CELL 1414$_1$
OUTPUT INTERFACE 118
RECEIVER 1450$_j$
CPU 1400
INPUT INTERFACE 116
TRANSMITTER 1440

FIG. 15

TOTO90 "00802860

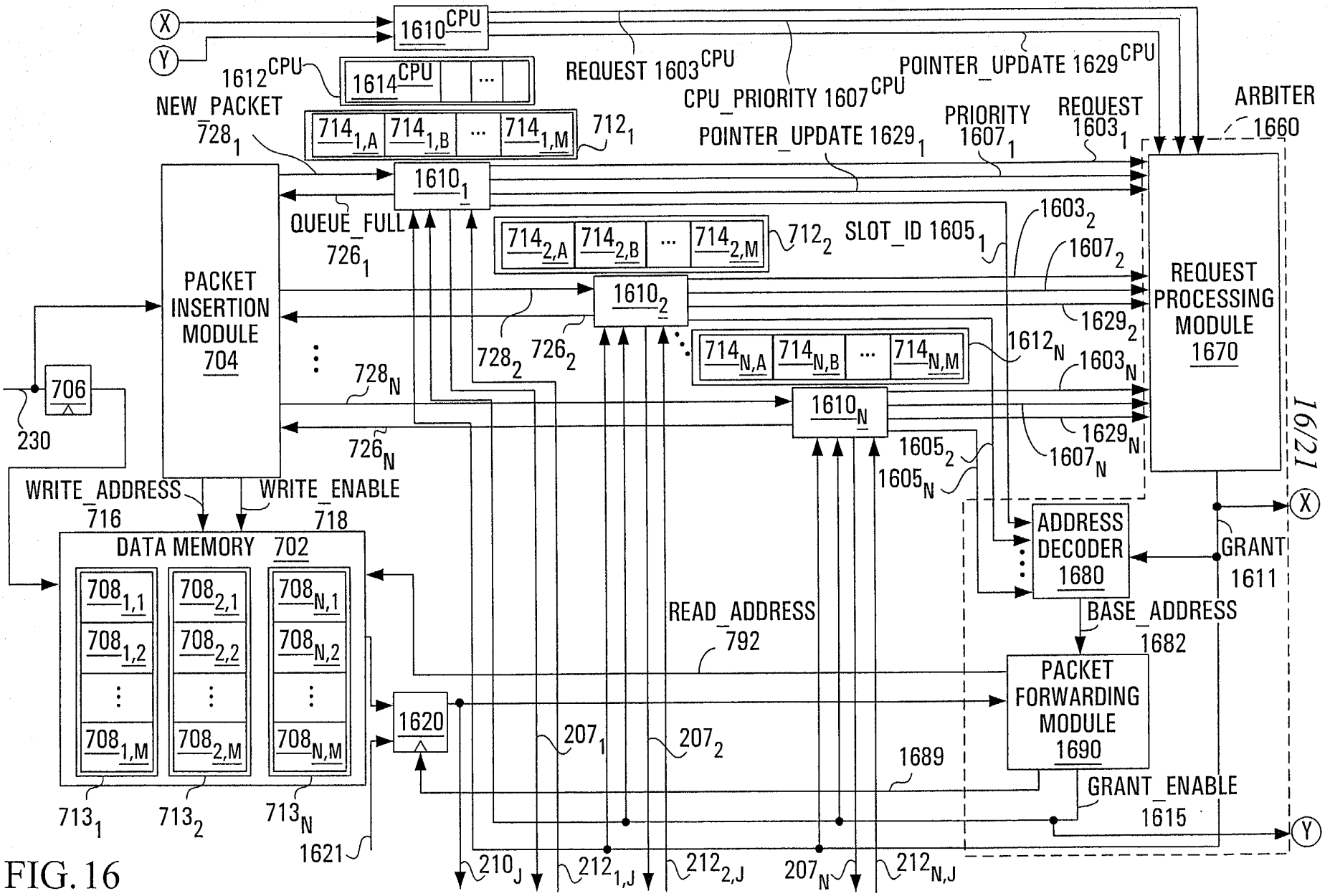


FIG. 16

FIG. 17A

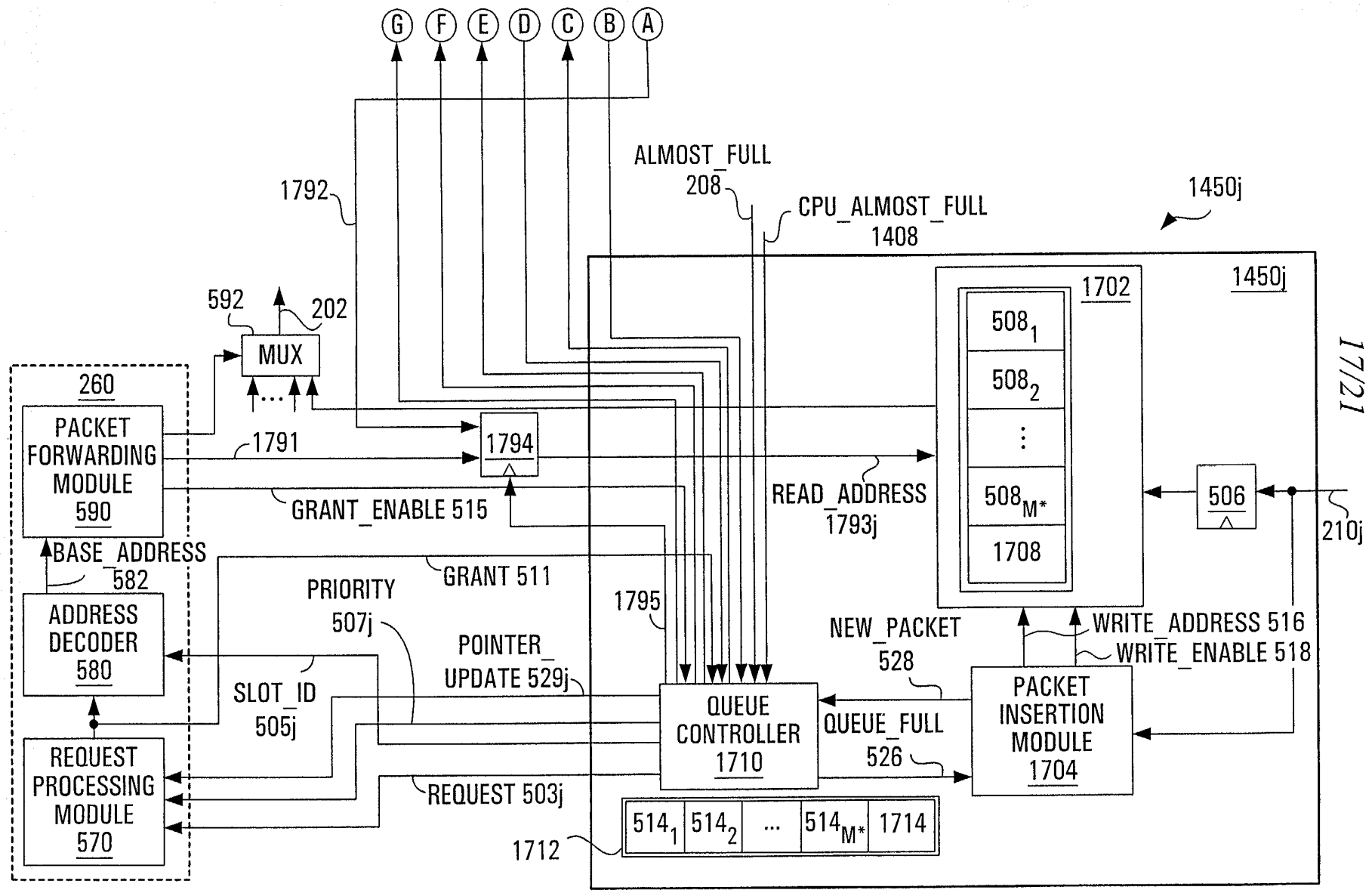
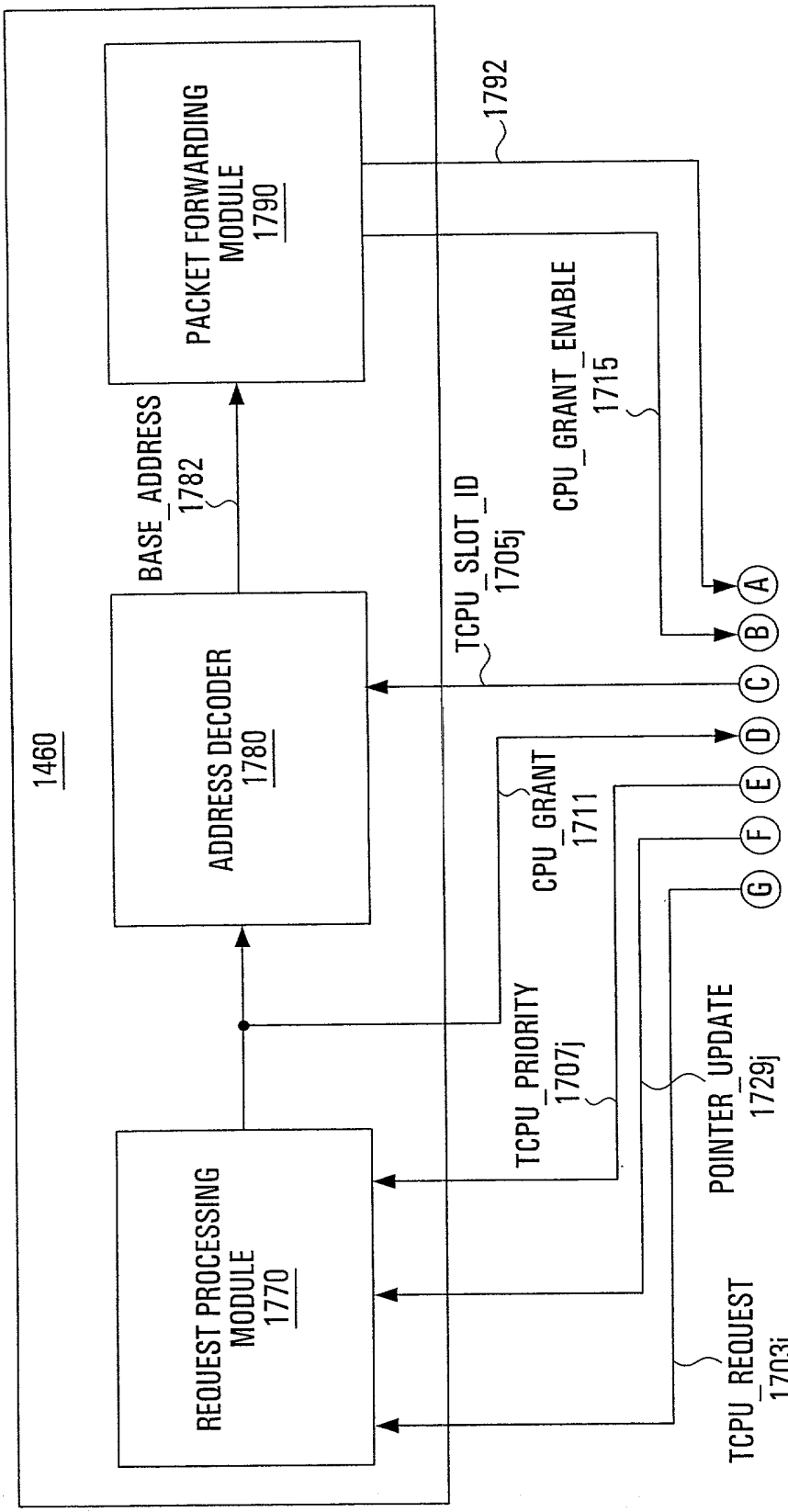

G
F
E
D
C
B
A
ALMOST_FULL
208
1792
CPU_ALMOST_FULL
1408
1450j
1702
1450j
592
202
MUX
260
PACKET FORWARDING MODULE 590
1791
1794
GRANT_ENABLE 515
READ_ADDRESS 1793j
506
210j
BASE_ADDRESS 582
GRANT 511
PRIORITY 507j
1795
ADDRESS DECODER 580
SLOT_ID 505j
POINTER_UPDATE 529j
NEW_PACKET 528
WRITE_ADDRESS 516
WRITE_ENABLE 518
QUEUE CONTROLLER 1710
QUEUE_FULL 526
PACKET INSERTION MODULE 1704
REQUEST PROCESSING MODULE 570
REQUEST 503j
1712
1714
17/21

FIG. 17B


1460
PACKET FORWARDING MODULE 1790
1792
BASE_ADDRESS 1782
ADDRESS DECODER 1780
TCPU_SLOT_ID 1705j
CPU_GRANT_ENABLE 1715
CPU_GRANT 1711
TCPU_PRIORITY 1707j
POINTER_UPDATE 1729j
REQUEST PROCESSING MODULE 1770
TCPU_REQUEST 1703j
A
B
C
D
E
F
G

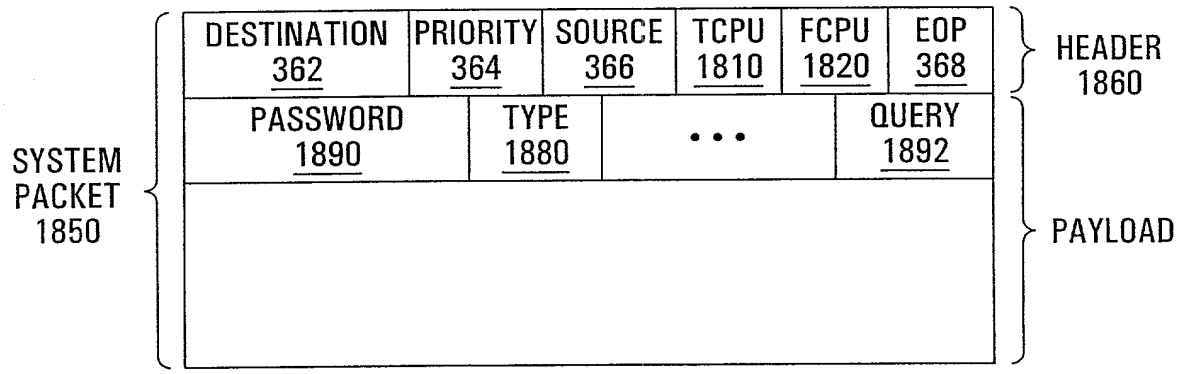


FIG. 18

Patent Application Publication

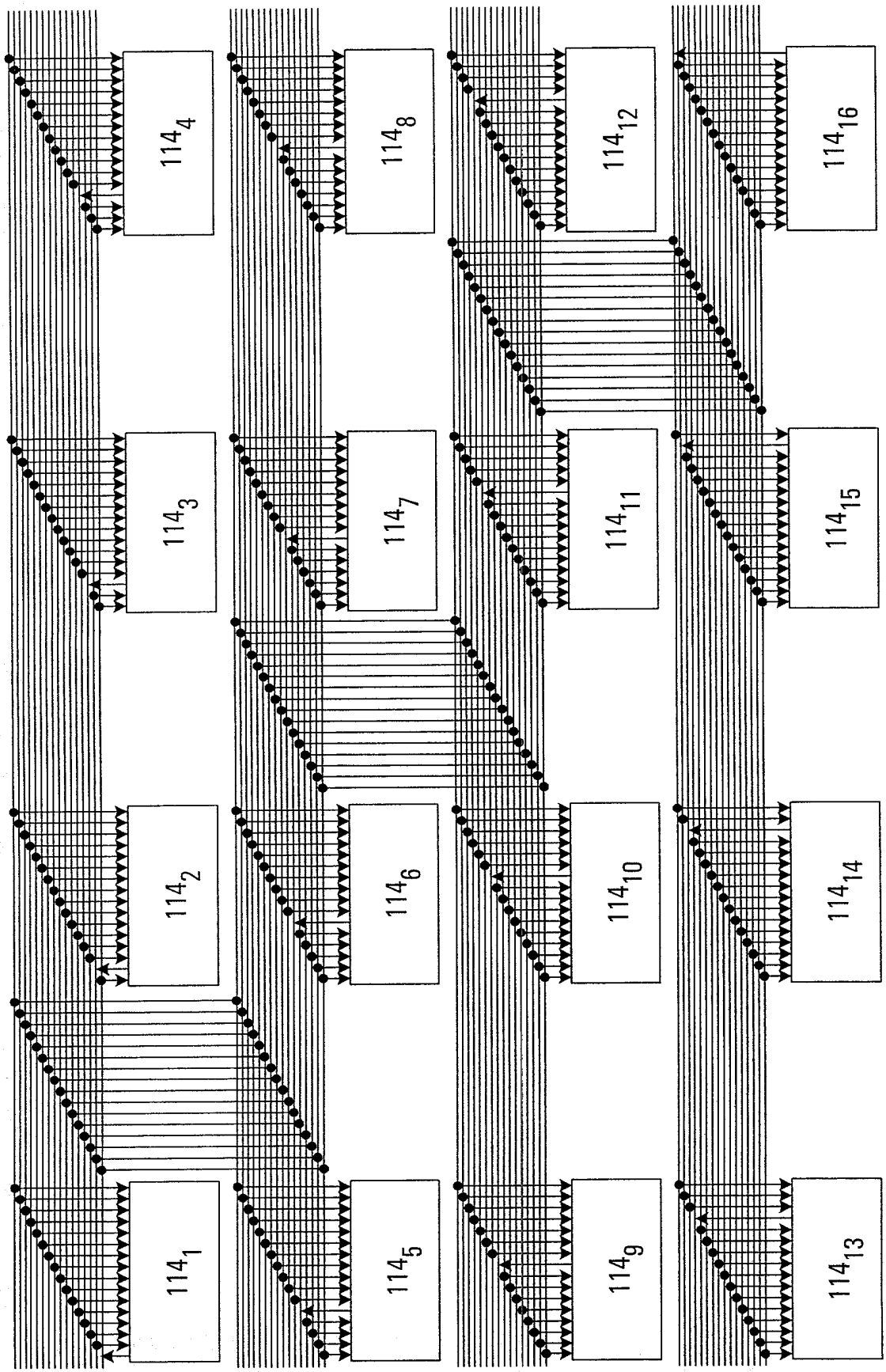

114_1
114_2
114_3
114_4
114_5
114_6
114_7
114_8
114_9
114_{10}
114_{11}
114_{12}
114_{13}
114_{14}
114_{15}
114_{16}

FIG. 19

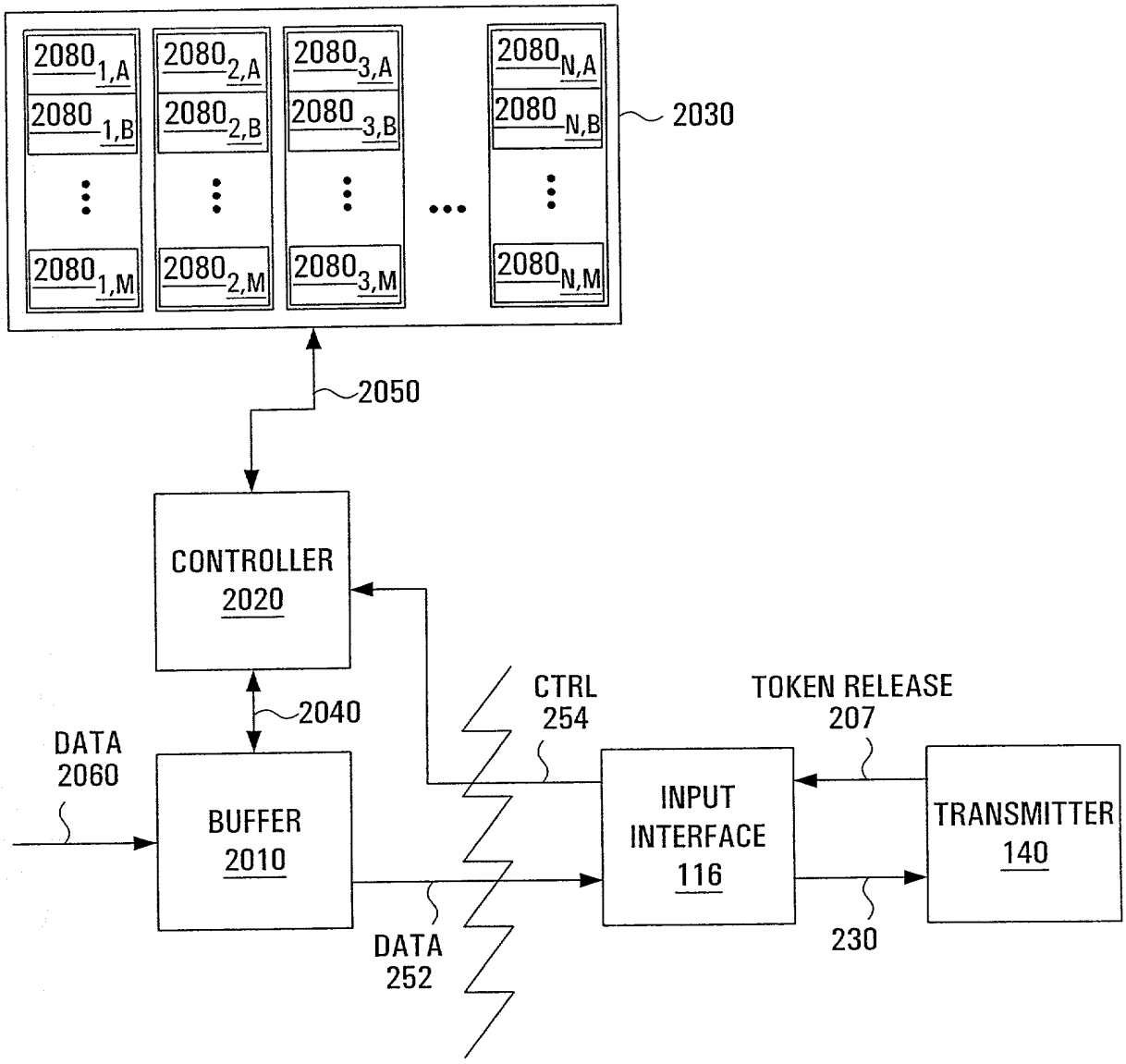

2080 1,A
2080 2,A
2080 3,A
2080 N,A
2080 1,B
2080 2,B
2080 3,B
2080 N,B
2080 1,M
2080 2,M
2080 3,M
2080 N,M
2030
2050
CONTROLLER
2020
2040
DATA
2060
BUFFER
2010
CTRL
254
TOKEN RELEASE
207
INPUT
INTERFACE
116
TRANSMITTER
140
DATA
252
230

FIG. 20